DSG-NPS R&D Meeting Minutes

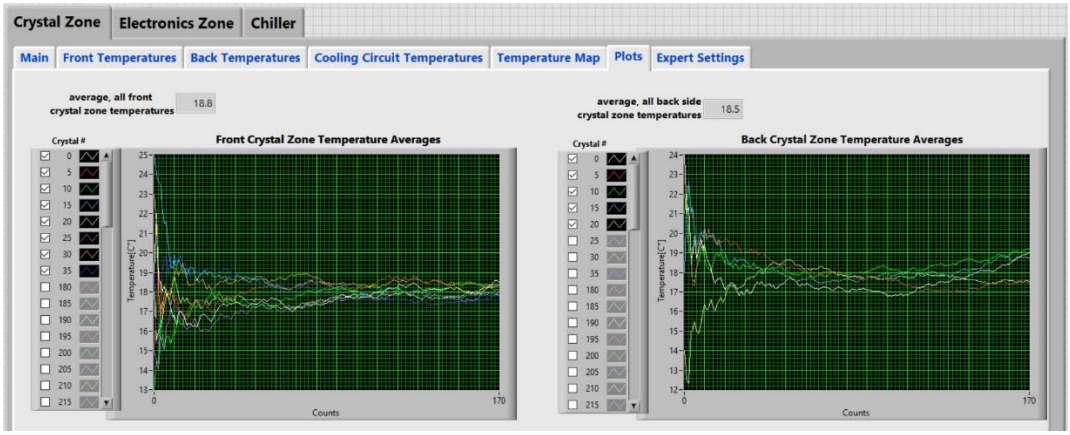
Date: July 13, 2021
Time: 11:00AM – 12:00 PM

Attendees: Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, and Marc McMullen

1. Hardware interlock system development

Mary Ann Antonioli, Peter Bonneau, and Aaron Brown

1. Reviewed progress on the LabVIEW front panel Mary Ann Antonioli is developing for the hardware monitoring system program
    - On the *Plots* tab, added two indicators, one for each crystal zone, that display the averages of all 56 average temperatures; code to display standard deviation averages is in progress

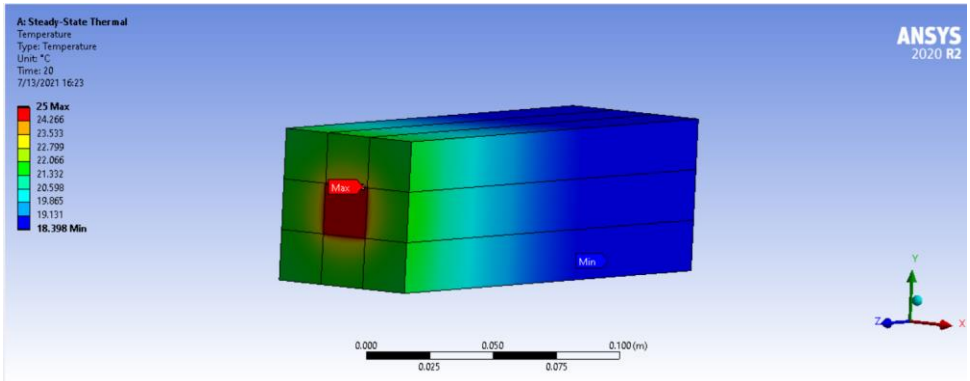


Screenshot of LabVIEW front panel for hardware interlock monitoring system program showing *Plots* tab

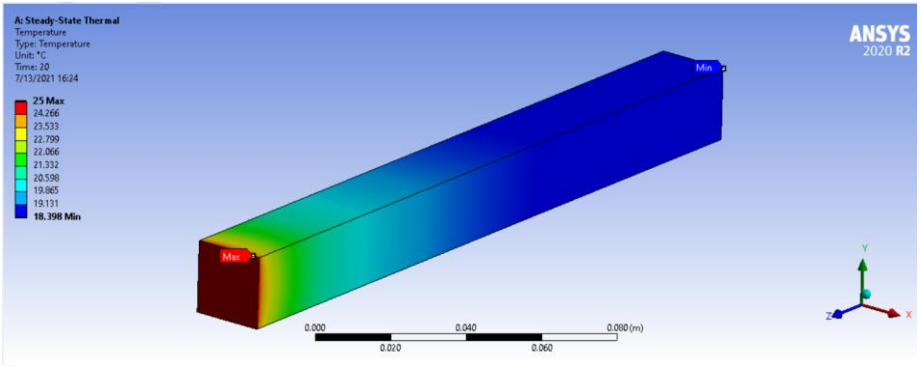
2. Thermal analysis and Ansys simulation

Aaron Brown

1. Reviewed Ansys thermal simulation of 3x3 block of $PbWO_4$ crystals
    - A temperature of 25° C was applied to the front of the central crystal
    - A thermal conductivity of 2.4 $Wm^{-1}K^{-1}$ was applied in the *x*- and *y*-directions and of 2.0 $Wm^{-1}K^{-1}$ in the *z*-direction



Thermal simulation of 3x3 cube of $PbWO_4$ crystals with 25° C applied to face of central crystal

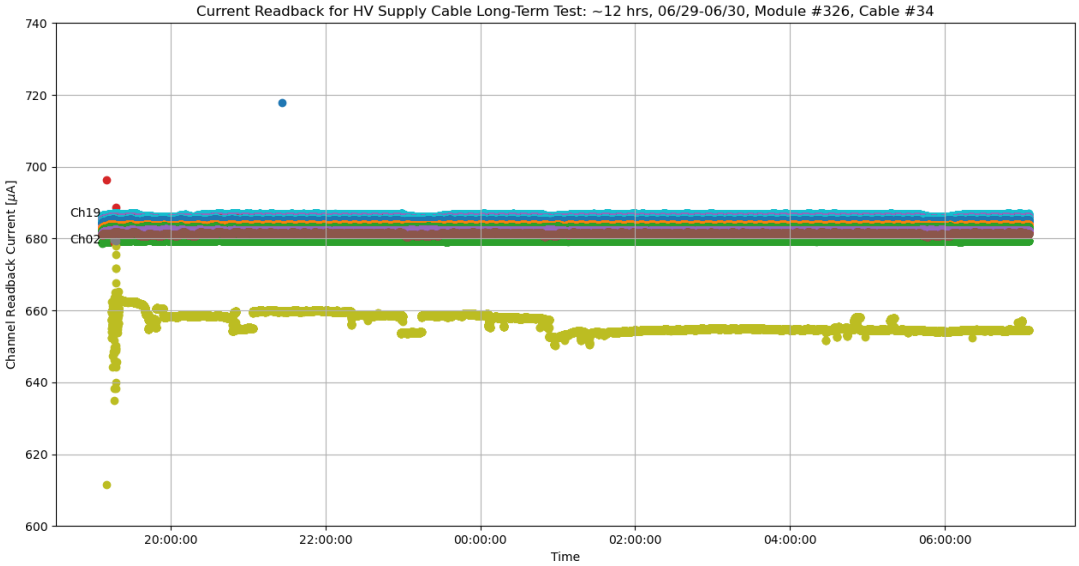


Central crystal of 3x3 cube of $PbWO_4$ with 25° C applied to its face

3. HV supply cable testing

Peter Bonneau, Aaron Brown, Brian Eng, George Jacobs, Mindy Leffel, and Marc McMullen

1. Long-term cable testing, with load, in progress
   - Cable #34, channel #8 will be repaired



Plot of retest of cable #34; channel #8 is still unstable

2. Researching appropriate hot glue to use for potting Radiall connector
   - Will contact CAEN for suggestion, have located a substitute hot glue
3. Will contact CAEN technical support for pins that can be used to test cable with Radiall connector at one end and flying leads replacing the Samtec end
   - A voltage calibrator will provide ~10 V to the Radiall end and the voltage will be monitored using a DMM at the Samtec end